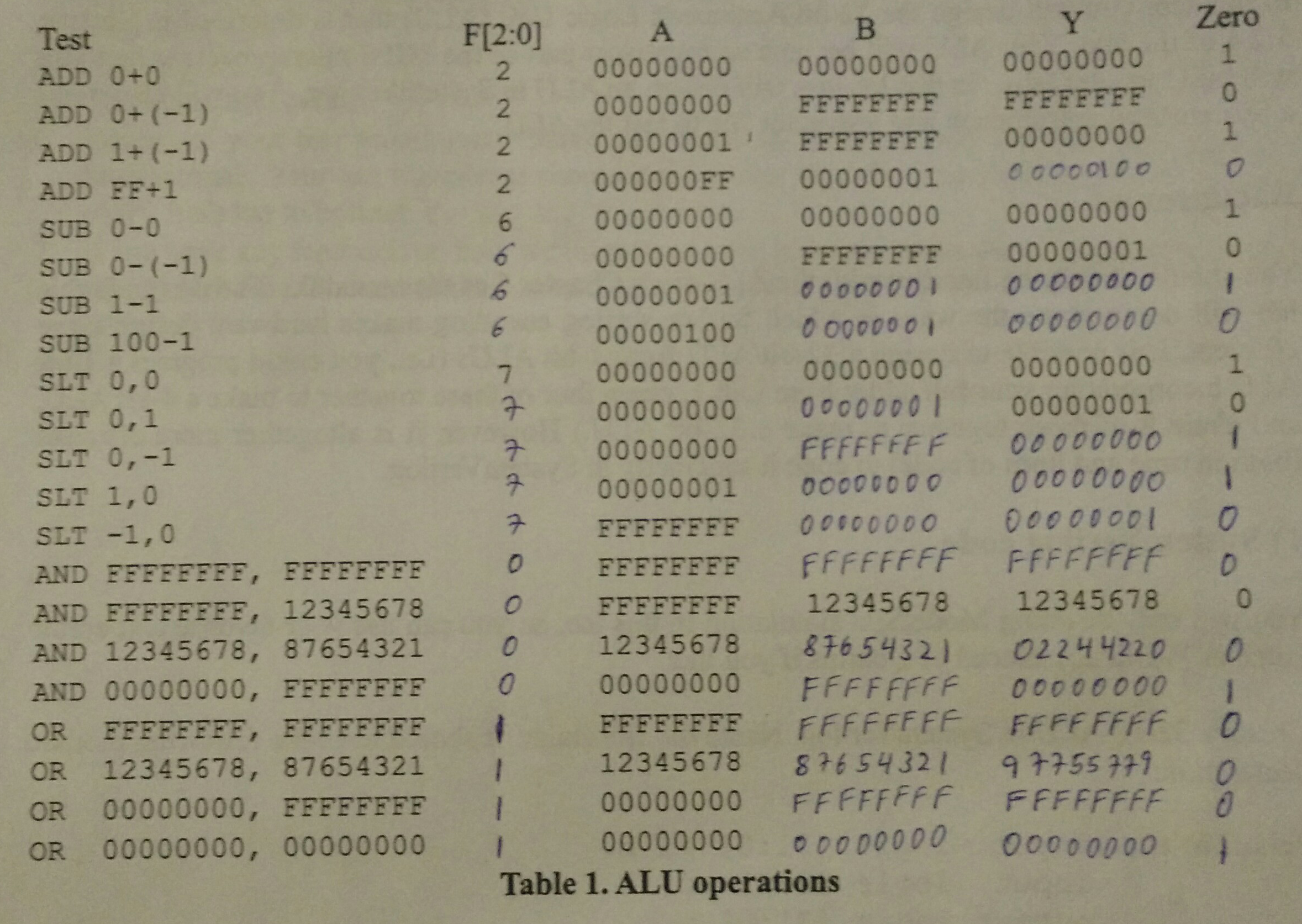
**Making a 32-bit ALU**

Time worked on lab: 3 hours

**Table of test vectors:**



**Alu.sv :**

module alu (input logic [31:0] a,input logic [31:0] b,input logic [2:0] f,

output logic [31:0] y,

output logic zero);

assign zero = (y==0);

always @(f, a, b) begin

case (f)

0: y<= a & b;

1: y<= a | b;

2: y<= a + b;

4: y<= a & (~b);

5: y<= a | (~b);

6: y<= a - b;

7: y<= a < b? 1: 0;

default: y<= 0;

endcase

end

endmodule

always\_comb begin if(y==8'h00000000) zero=1;

else

zero=0;

end

endmodule

**Alu.tv:**

2\_00000000\_00000000\_00000000\_1

2\_00000000\_FFFFFFFF\_FFFFFFFF\_0

2\_00000001\_FFFFFFFF\_00000000\_1

2\_000000FF\_00000001\_00000100\_0

6\_00000000\_00000000\_00000000\_1

6\_00000000\_FFFFFFFF\_00000001\_0

6\_00000001\_00000001\_00000000\_1

6\_00000100\_00000001\_000000FF\_0

7\_00000000\_00000000\_00000000\_1

7\_00000000\_00000001\_00000001\_0

7\_00000000\_FFFFFFFF\_00000000\_1

7\_00000001\_00000000\_00000000\_1

7\_FFFFFFFF\_00000000\_00000001\_0

0\_FFFFFFFF\_FFFFFFFF\_FFFFFFFF\_0

0\_FFFFFFFF\_12345678\_12345678\_0

0\_12345678\_87654321\_02244220\_0

0\_00000000\_FFFFFFFF\_00000000\_1

1\_FFFFFFFF\_FFFFFFFF\_FFFFFFFF\_0

1\_12345678\_87654321\_97755779\_0

1\_00000000\_FFFFFFFF\_FFFFFFFF\_0

1\_00000000\_00000000\_00000000\_1

**testbench.sv:**

module testbench();

logic clk, reset;

logic [31:0] a, b, yexpected;

logic [2:0] f, junk2;

logic y, junk1, zero, zeroexpected;

logic [31:0] vectornum,errors;

logic [104:0] testvectors [1000:0];

alu dut(a,b,f,y,zero);

always

begin

clk = 1; #50 ; clk = 0; #50;

end

initial

begin

$readmemh("alu.tv", testvectors);

vectornum = 0; errors = 0;

reset = 1; #50 ; reset = 0;

end

always @ (posedge clk)

begin

#1; {junk1, f, a , b, yexpected,junk2,zeroexpected} = testvectors[vectornum];

end

always @ (negedge clk)

if(~reset) begin

if( y !== yexpected ) begin

$display ("Error: inputs = %b", { a, b, f} );

$display( "outputs = %b (%b expected)", y, yexpected);

errors = errors +1;

end

vectornum = vectornum +1;

if (testvectors[vectornum] === 4'bx) begin

$display("%d tests completed with %d errors", vectornum, errors);

$finish;

end

end

endmodule

**waveforms:**

